

INN900D350B

1. General description

900V GaN-on-Silicon Enhancement-mode Power Transistor in Dual Flat No-lead package (DFN) with 8 mm × 8 mm size

2. Features

- Enhancement mode transistor-Normally off power switch
- Ultra high switching frequency
- No reverse-recovery charge
- Low gate charge, low output charge
- Qualified for industrial applications according to JEDEC Standards
- ESD safeguard
- RoHS, Pb-free, REACH-compliant

3. Applications

- AHB/LLC/ACF Converter for Fast battery charger
- QR Flyback Converter for Fast battery charger
- Optimized to withstand high voltage transients in unstable mains network

4. Key performance parameters

Table 1 Key performance parameters at $T_j = 25\text{ }^{\circ}\text{C}$

Parameter	Value	Unit
$V_{DS,max}$	900	V
$R_{DS(on),max} @ V_{GS} = 6\text{ V}$	350	m Ω
$Q_{G,typ} @ V_{DS} = 400\text{ V}$	1.5	nC
$I_{D,pulse}$	10	A
$Q_{OSS} @ V_{DS} = 400\text{ V}$	16.5	nC
$Q_{rr} @ V_{DS} = 400\text{ V}$	0	nC

5. Pin information

Table 2 Pin information

Gate	Drain	Kelvin Source	Source
8	1, 2, 3, 4	7	5, 6, 9

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN900D350B	DFN 8X8	90D350B

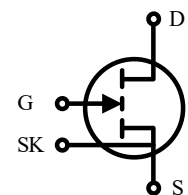
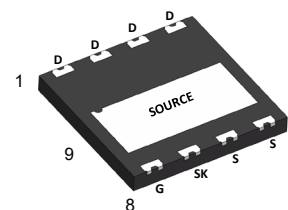
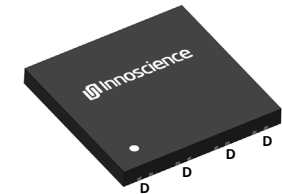


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6. Maximum ratings

at $T_j = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscence sales office.

Table 4 Maximum ratings

Parameter	Symbol	Values	Unit	Note/Test Condition
Drain source voltage	$V_{DS,max}$	900	V	$V_{GS} = 0\text{ V}$, $T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Continuous current, drain source	I_D	6	A	$T_c = 25\text{ }^{\circ}\text{C}$
Pulsed current, drain source ¹	$I_{D,pulse}$	10	A	$T_c = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Pulsed current, drain source ¹	$I_{D,pulse}$	6	A	$T_c = 125\text{ }^{\circ}\text{C}$; $V_{GS} = 6\text{ V}$; $t_{PULSE} = 10\text{ }\mu\text{s}$
Gate source voltage, continuous ²	V_{GS}	-1.4 to +7	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$
Gate source voltage, pulsed	$V_{GS,pulse}$	-20 to +10	V	$T_j = -55\text{ }^{\circ}\text{C}$ to $150\text{ }^{\circ}\text{C}$; $t_{PULSE} = 50\text{ ns}$, $f = 100\text{ kHz}$; open drain
Power dissipation	P_{tot}	59	W	$T_c = 25\text{ }^{\circ}\text{C}$
Operating temperature	T_j	-55 to +150	$^{\circ}\text{C}$	
Storage temperature	T_{stg}	-55 to +150	$^{\circ}\text{C}$	

¹ Limit was extracted from characterization test, not measured during production

² The minimum V_{GS} is clamped by ESD protection circuit, as shown in Figure 10

7. Thermal characteristics

Table 5 Thermal characteristics

Parameter	Symbol	Values	Unit	Note/Test Condition
Thermal resistance, junction-ambient	R_{thJA}^1	67	°C/W	
Thermal resistance, junction-case	R_{thJC}	2.11	°C/W	
Maximum reflow soldering temperature	T_{sold}	260	°C	MSL3

1. R_{thJA} is determined with the device mounted on one square inch of copper pad, single layer 2oz copper on FR4 board.

8. Electric characteristics

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

Table 6 Static characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(th)}$	1.2	1.7	2.5	V	$I_D = 7.4\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	1.6	-		$I_D = 7.4\text{ mA}$; $V_{DS} = V_{GS}$; $T_j = 150\text{ }^{\circ}\text{C}$
Drain-source leakage current	I_{DSS}	-	0.6	15	μA	$V_{DS} = 720\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	5	-		$V_{DS} = 720\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	40	-	μA	$V_{GS} = 6\text{ V}$; $V_{DS} = 0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	265	350	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 2.2\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$
		-	583	-	$\text{m}\Omega$	$V_{GS} = 6\text{ V}$; $I_D = 2.2\text{ A}$; $T_j = 150\text{ }^{\circ}\text{C}$
Gate resistance	R_G	-	8	-	Ω	$f = 5\text{ MHz}$; open drain

Table 7 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	54	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Output capacitance	C_{oss}	-	21	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Reverse transfer Capacitance	C_{rss}	-	0.2	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 400\text{ V}$; $f = 100\text{ kHz}$
Effective output capacitance, energy related ¹	$C_{o(er)}$	-	29	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Effective output capacitance, time related ²	$C_{o(tr)}$	-	40	-	pF	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$
Output charge	Q_{oss}	-	16.5	-	nC	$V_{GS} = 0\text{ V}$; $V_{DS} = 0\text{ to }400\text{ V}$

- $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 400 V
- $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 400 V

Table 8 Gate charge characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Gate charge	Q_G	-	1.5	-	nC	$V_{GS} = 0 \text{ to } 6 \text{ V}; V_{DS} = 400 \text{ V}; I_D = 2.2 \text{ A}$
Gate-source charge	Q_{GS}	-	0.12	-	nC	
Gate-drain charge	Q_{GD}	-	0.5	-	nC	
Gate Plateau Voltage	V_{Plat}	-	2.2	-	V	$V_{DS} = 400 \text{ V}; I_D = 2.2 \text{ A}$

Table 9 Reverse conduction characteristics

Parameter	Symbol	Values			Unit	Note/Test Condition
		Min.	Typ.	Max.		
Source-Drain reverse voltage	V_{SD}	-	2.6	-	V	$V_{GS} = 0 \text{ V}; I_S = 2.2 \text{ A}$
Pulsed current, reverse	$I_{S,pulse}$	-	-	14	A	$V_{GS} = 6 \text{ V}; t_{PULSE} = 10 \mu s$
Reverse recovery charge	Q_{rr}	-	0	-	nC	$I_S = 2.2 \text{ A}; V_{DS} = 400 \text{ V}$
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

9. Electric characteristics diagrams

at $T_j = 25\text{ }^{\circ}\text{C}$, unless specified otherwise

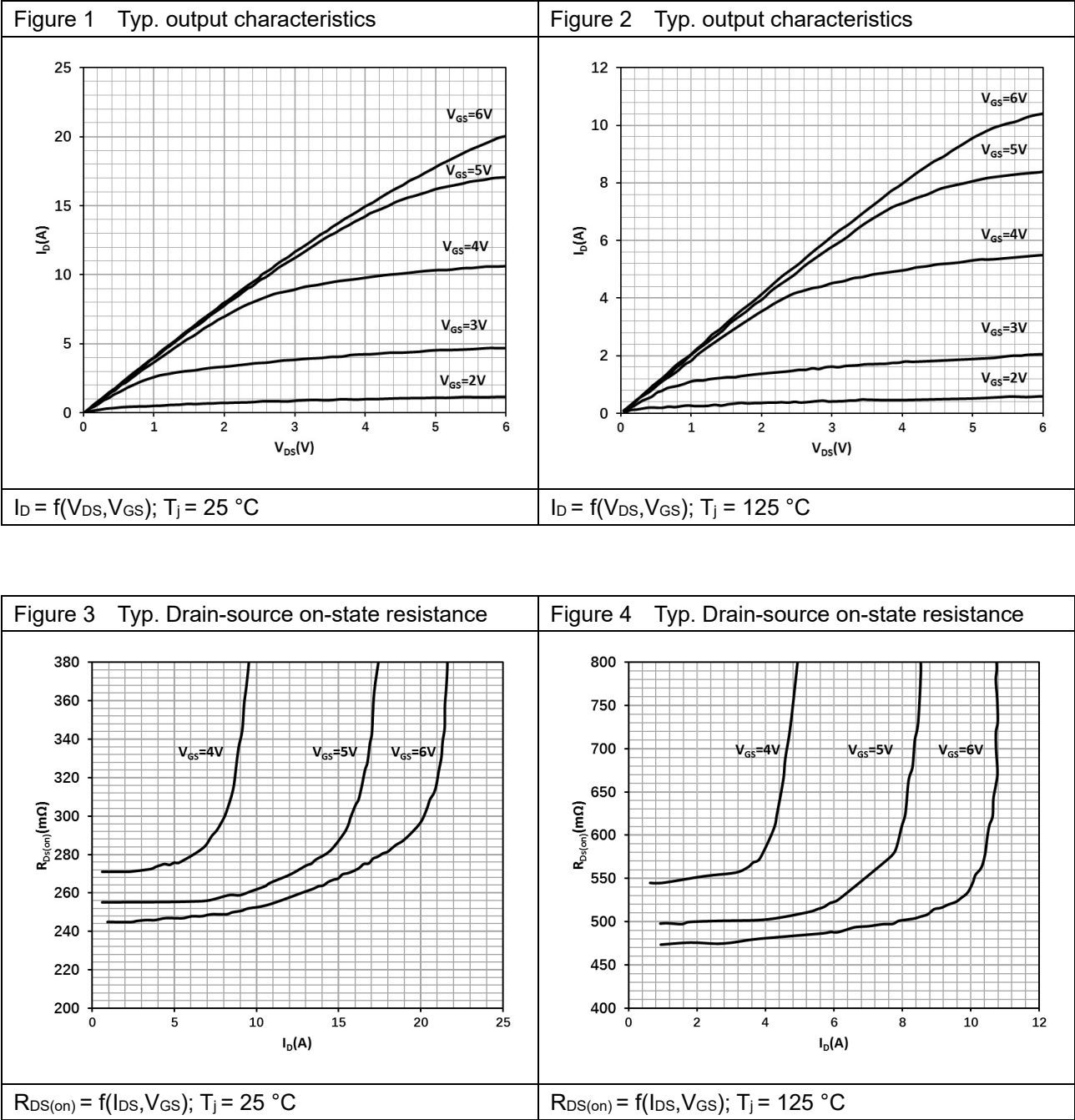
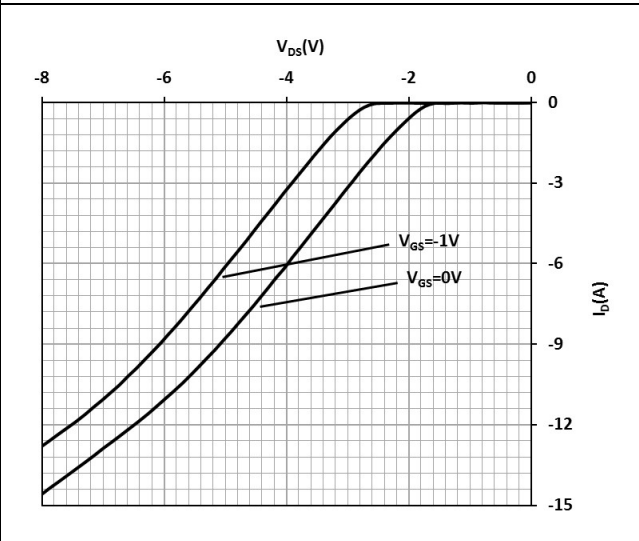
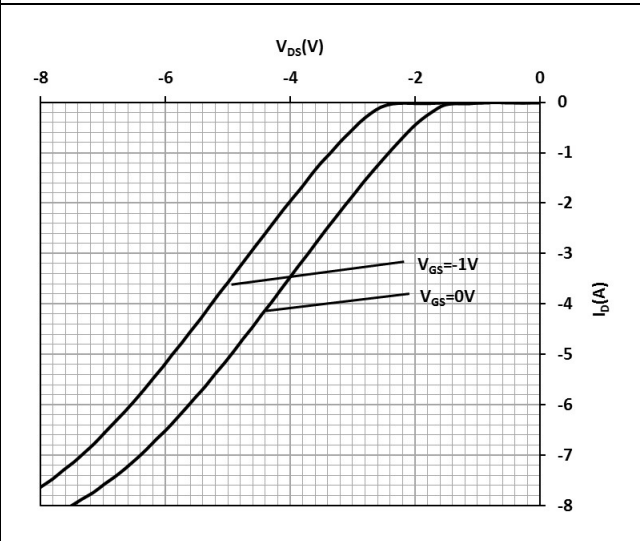


Figure 5 Typ. channel reverse characteristics



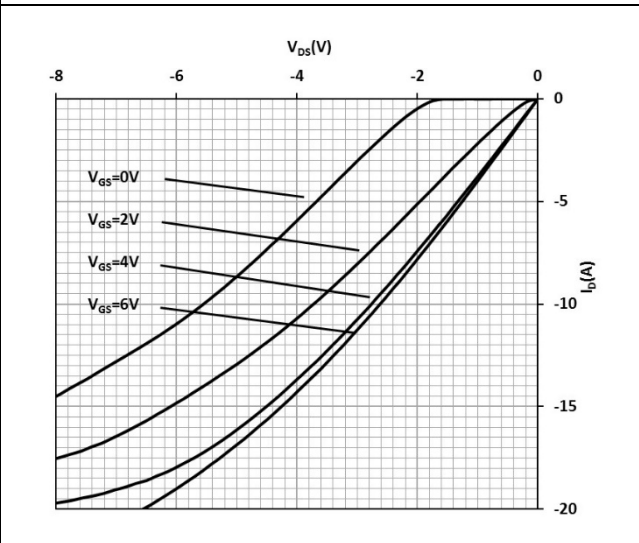
$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^{\circ}\text{C}$

Figure 6 Typ. channel reverse characteristics



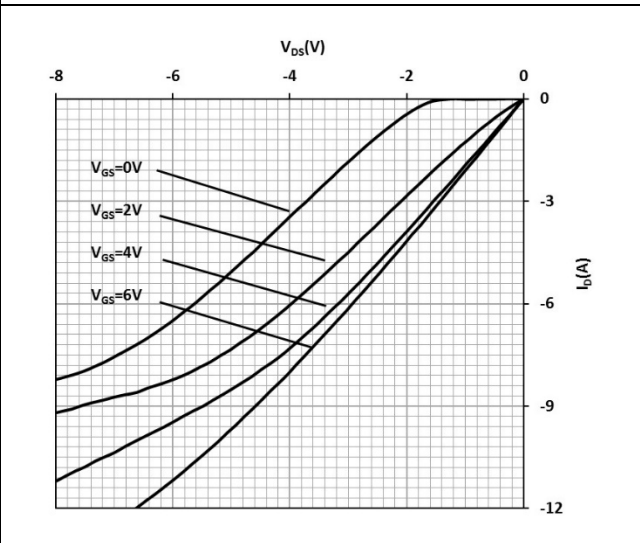
$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^{\circ}\text{C}$

Figure 7 Typ. channel reverse characteristics



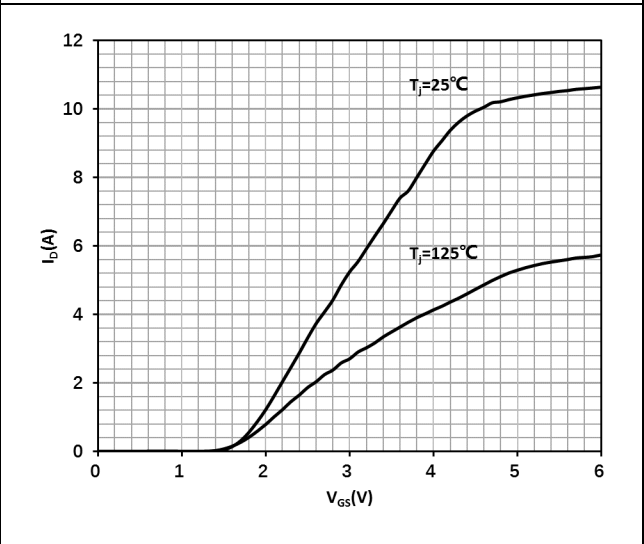
$I_D = f(V_{DS}, V_{GS}); T_J = 25\text{ }^{\circ}\text{C}$

Figure 8 Typ. channel reverse characteristics



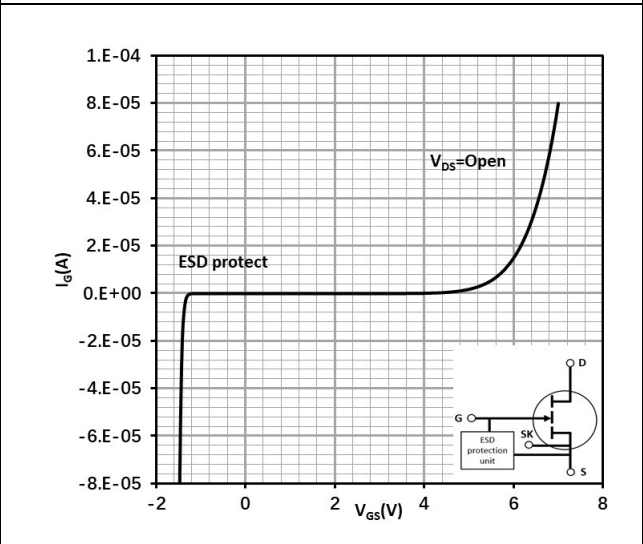
$I_D = f(V_{DS}, V_{GS}); T_J = 125\text{ }^{\circ}\text{C}$

Figure 9 Typ. transfer characteristics



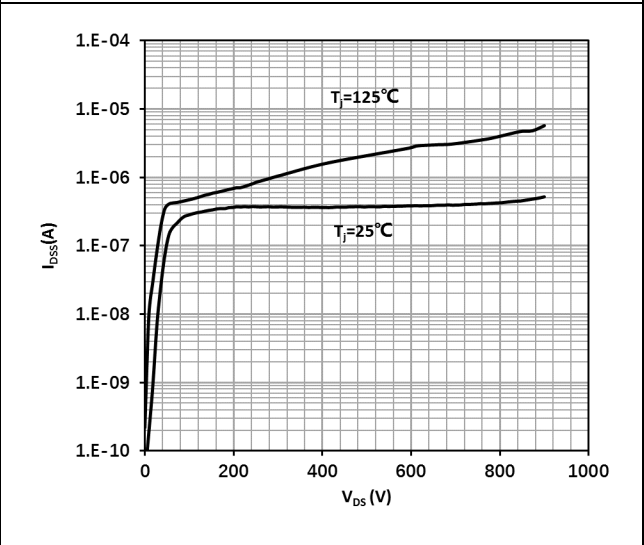
$I_D = f(V_{GS}); V_{DS} = 3\text{ V}$

Figure 10 Typ. Gate-to-Source leakage



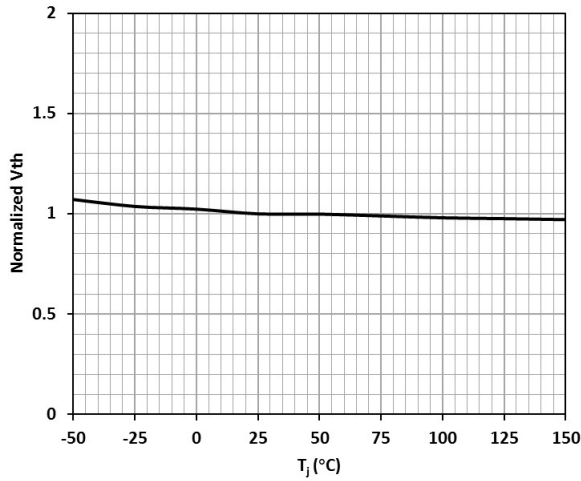
$I_G = f(V_{GS}); I_G$ reverse turn on by ESD unit

Figure 11 Drain-source leakage characteristics



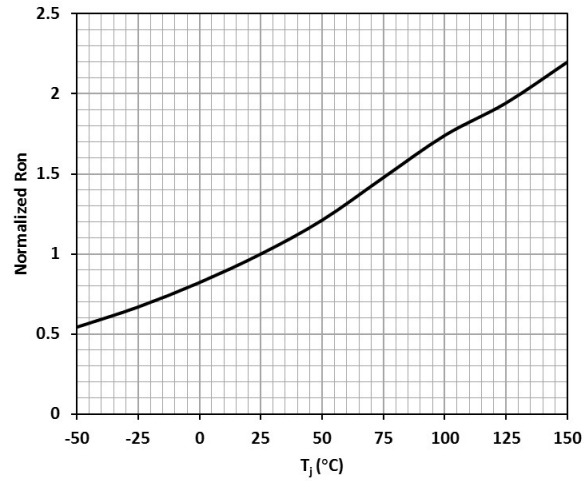
$I_{DSS} = f(V_{DS}); V_{GS} = 0\text{ V}$

Figure 12 Gate threshold voltage



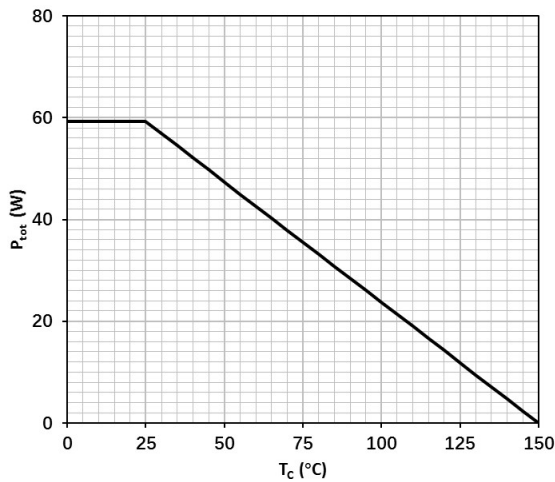
$$V_{TH} = f(T_j); V_{GS} = V_{DS}; I_D = 7.4 \text{ mA}$$

Figure 13 Drain-source on-state resistance



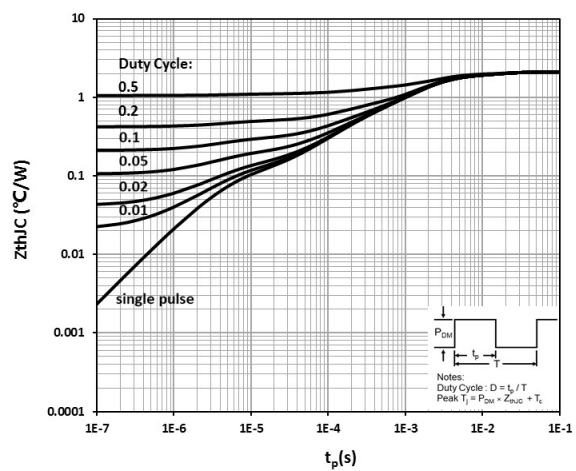
$$R_{DS(on)} = f(T_j); I_D = 2.2 \text{ A}; V_{GS} = 6 \text{ V}$$

Figure 14 Power dissipation



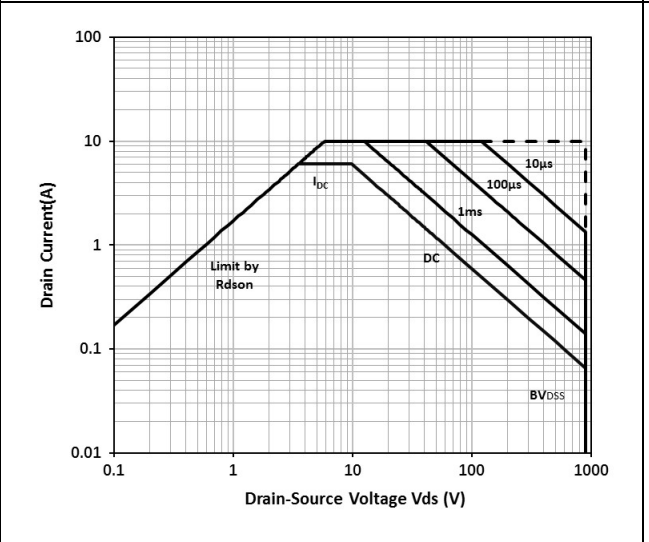
$$P_{tot} = f(T_c)$$

Figure 15 Max.transient thermal impedance



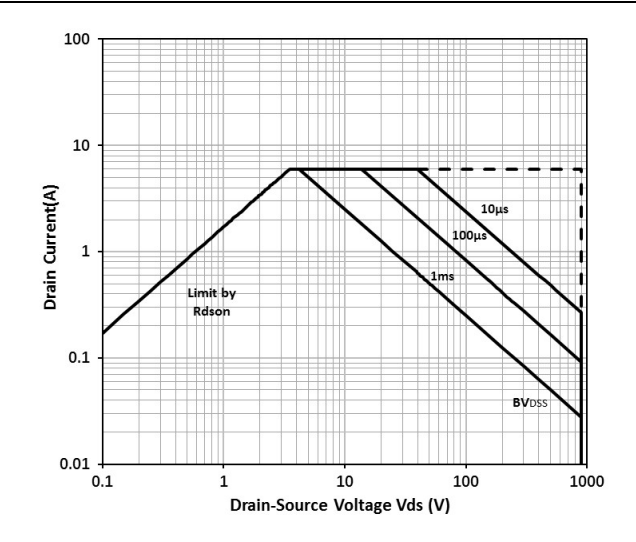
$$Z_{thJC} = f(t_p, D)$$

Figure 16 Safe operating area



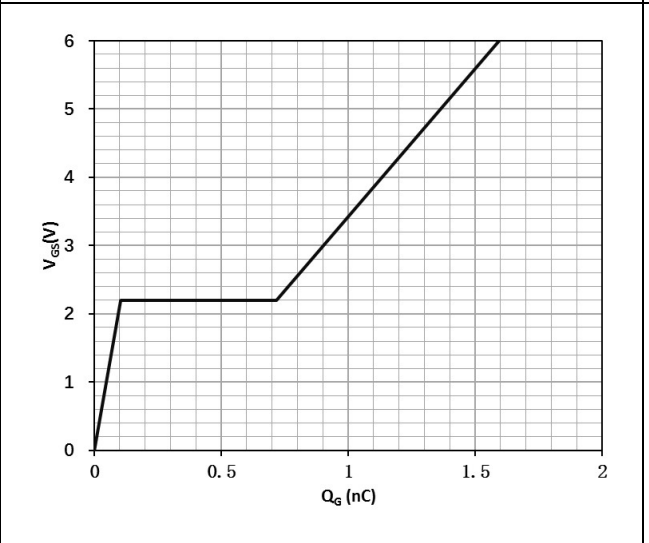
$I_D = f(V_{DS}); T_C = 25\text{ °C}$

Figure 17 Safe operating area



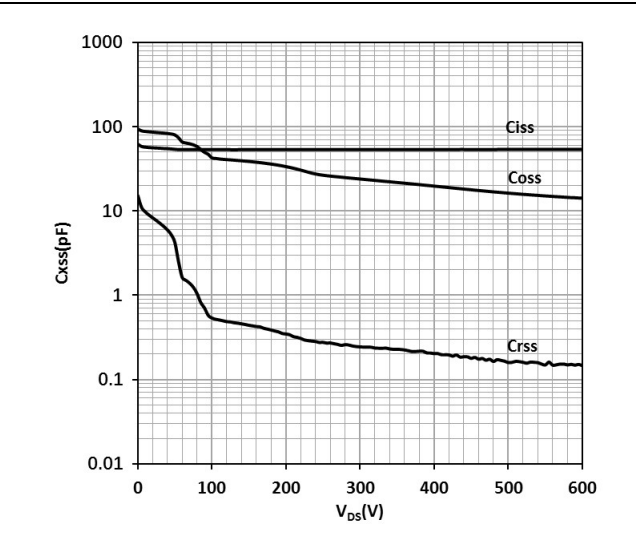
$I_D = f(V_{DS}); T_C = 125\text{ °C}$

Figure 18 Typ. gate charge



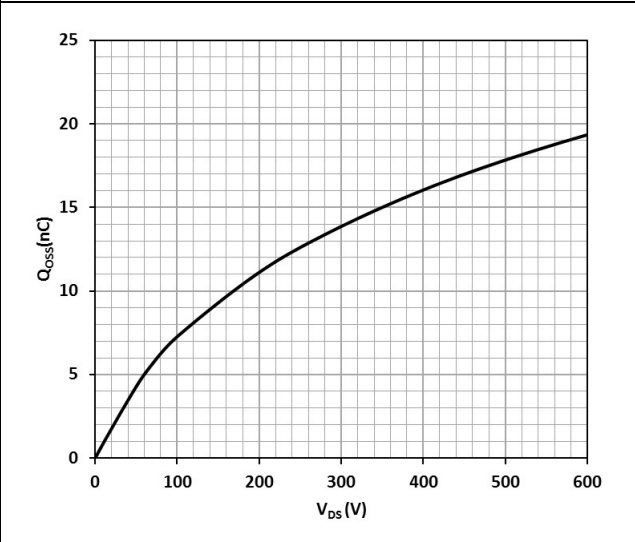
$V_{GS} = f(Q_G); V_{DCLINK} = 400\text{ V}; I_D = 2.2\text{ A}$

Figure 19 Typ. capacitances



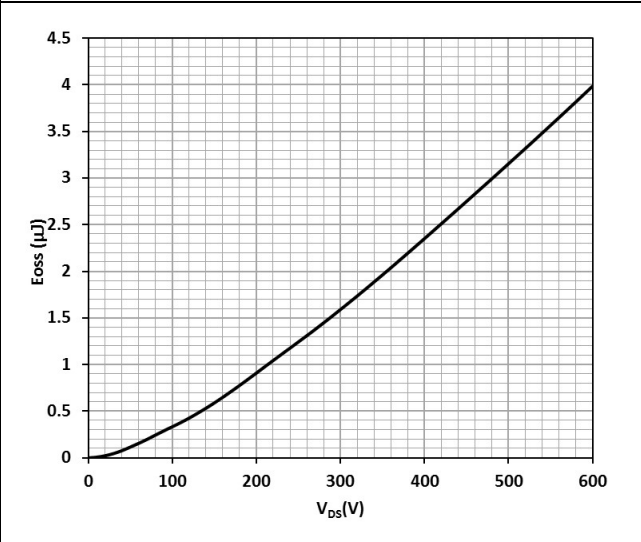
$C_{XSS} = f(V_{DS}); \text{Freq.} = 100\text{ kHz}$

Figure 20 Typ. output charge



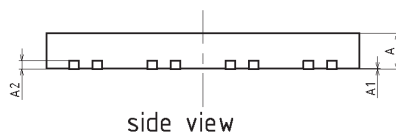
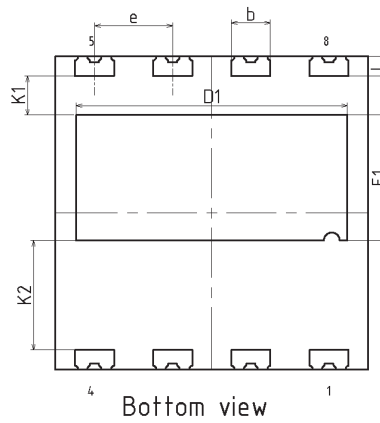
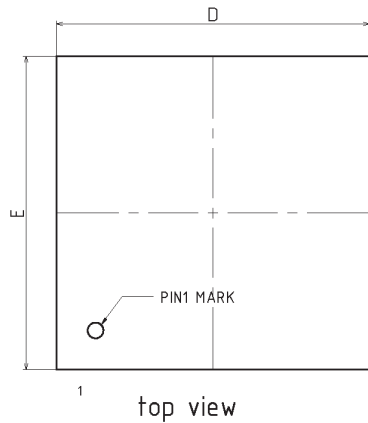
$Q_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

Figure 21 Typ. Coss stored Energy

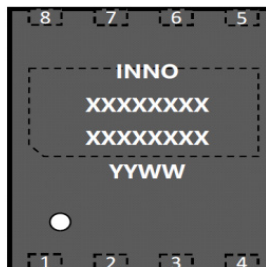


$E_{oss} = f(V_{DS}); \text{Freq.} = 100 \text{ kHz}$

10. Package outlines



SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
A2	0.203REF		
b	0.95	1.00	1.05
D	8.00 BSC		
D1	6.84	6.94	7.04
E	8.00 BSC		
E1	3.10	3.20	3.30
K1	0.90	1.00	1.10
K2	2.70	2.80	2.90
e	2.00 BSC		
L	0.40	0.50	0.60

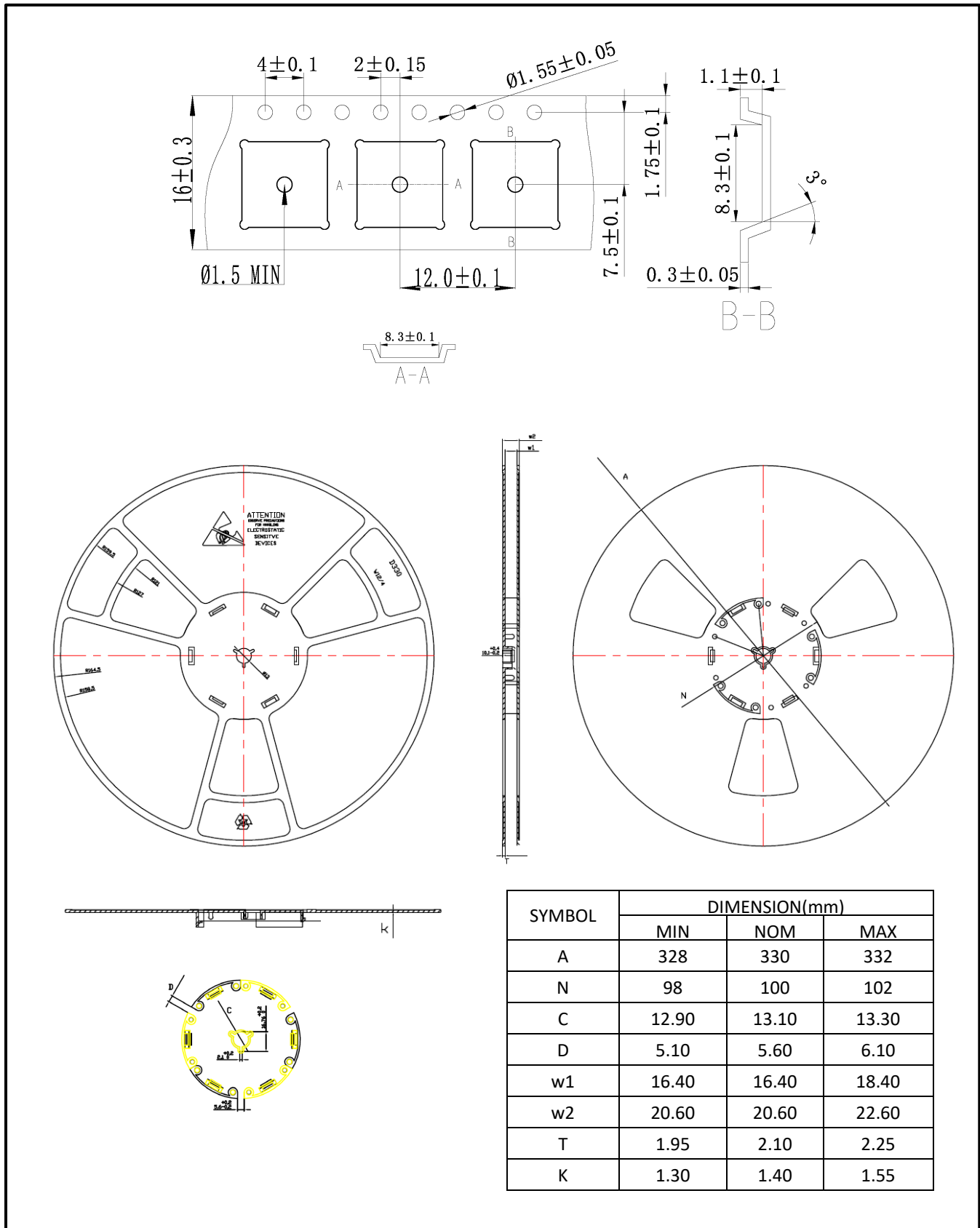


Row	Description	Example
Row1	Company name	INNO
Row2	Product code (In short)	XXXXXXX
Row3	ASSY lot No.	XXXXXXX
Row4	Date code	YYWW

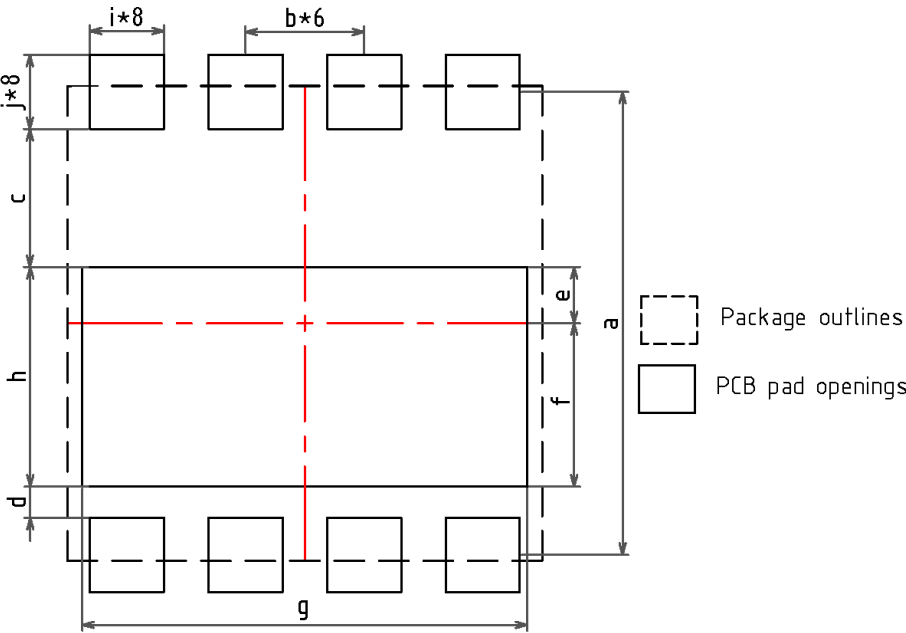
Notes:

- (1) Dimension and tolerance conform to ASME Y14.5-2009.
- (2) All dimension are in millimeters.
- (3) Lead coplanarity shall be 0.1 millimeters max.
- (4) Complies with JEDEC MO-229.
- (5) Drawing is not to scale.
- (6) Dimensions do not include mold protrusion.
- (7) Package outline exclusive of metal burr dimensions.

11. Reel information



12. Recommended PCB footprint



SYMBOL	DIMENSION	SYMBOL	DIMENSION
a	7.800	f	2.750
b	2.000	g	7.500
c	2.325	h	3.700
d	0.525	i	1.400
e	0.950	j	1.250

Notes:
(1) All dimension are in millimeters.
(2) Drawing is not to scale.

13.Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-06-04	1.0 version release

Important Notice

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